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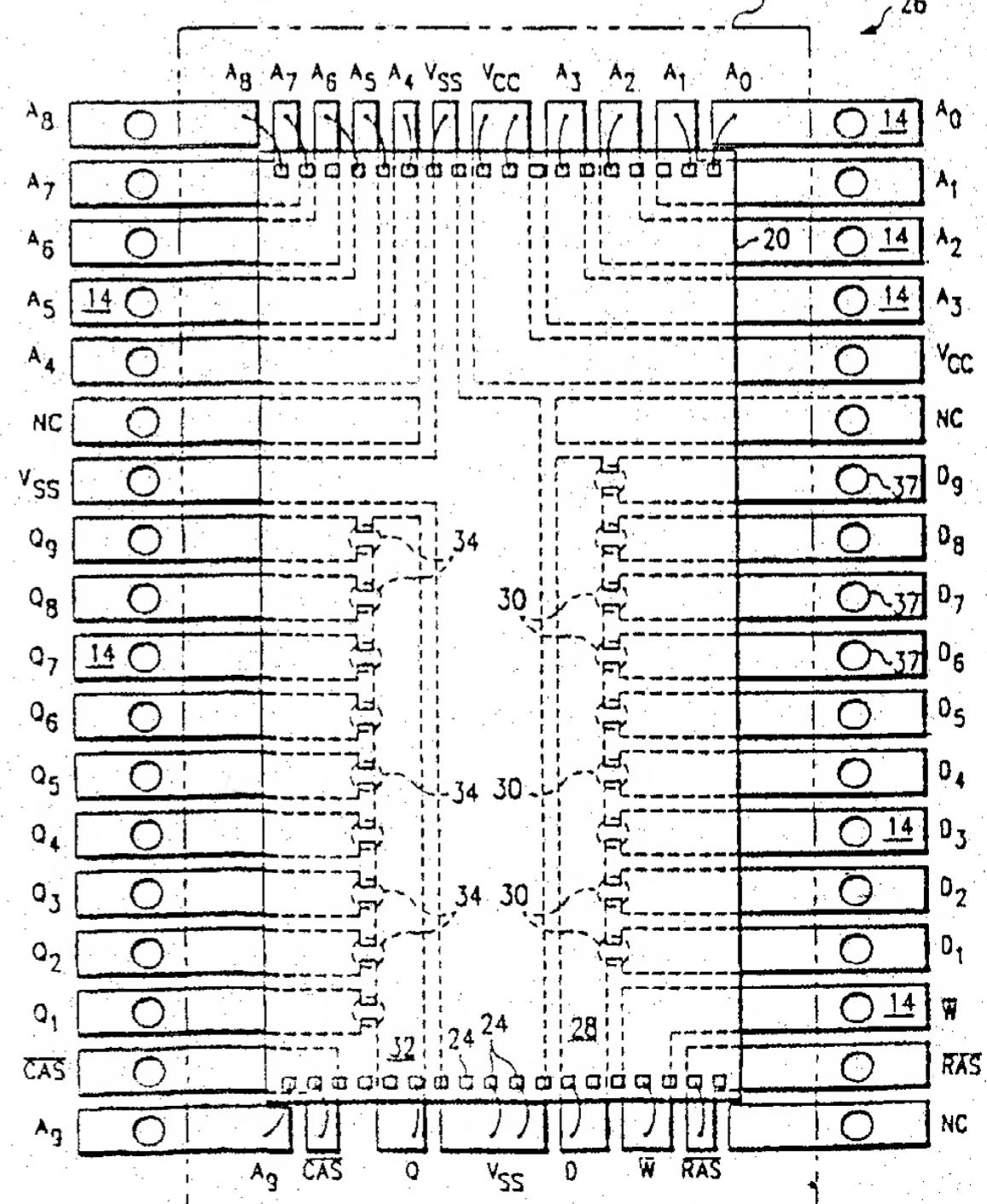
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(54) Title: HIGH DENSITY MEMORY AND METHOD OF FORMING THE SAME

(57) Abstract

A high density memory module (10) includes a plurality of subassemblies (12), each subassembly (12) including a memory circuit (20), a lead frame (26) having a plurality of leads (14) coupled to the memory circuit (20) and encapsulating material (13) surrounding the memory circuit (20) and lead frame (26) such that the leads (14) extend outwardly from the encapsulating material (13). The memory module (10) is easily assembled and provides high density storage capability with convective heat transfer to reduce the temperature within the stack of subassemblies (12). A single lead frame (26) may be selectively addressed for use with each subassembly (12) within the memory module (10).



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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS, search terms: memory module, subassembly, lead frame

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|-----------|--|-----------------------|
| x | US, A, 5,028,986 (Sugano et al.) 02 July 1991, col. 5, line 35 through col. 18, line 64. | 1-12 |

Further documents are listed in the continuation of Box C.

See patent family annex.

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DESCRIPTION

HIGH DENSITY MEMORY AND METHOD OF FORMING THE SAME

Technical Field

This invention relates in general to integrated circuits, and more particularly to a high density memory module.

Background Art

High speed digital processing systems often require large amounts of high speed memory. While mass memory devices, such as hard disks, are capable of storing large amounts of information, the speed associated with these devices is insufficient for many purposes. In many applications, speed considerations are satisfied by storing large amounts of information in semiconductor memory, such as dynamic random access memory (DRAM) and static random access memory (SRAM).

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1 Normally, semiconductor memory is packaged in DIPs (dual-inline
2 packages), ZIPs (Zip-Zag Inline Packages), SOJs (Small Outline J-leaded),
3 SIPs (single-inline packages), and SIMMs (single-inline memory module).
4 In these packaging options, the package itself is many times the size of the
5 semiconductor integrated circuit which performs the memory function.
6 Applications which need a large amount of memory or provide user-
7 upgradeable sockets for increasing the size of the memory often dedicate a
8 large area on the circuit board for the memory chips.

9 Currently, one megabit DRAMs are the industry standard memory
10 circuits, with four megabit memory circuits now reaching price parity with
11 the one megabit circuits. While board space is reduced by the improved
12 chip densities, the need for increased memory generally outpaces the speed
13 with which memory circuit densities are increased.

14 A prior art interim solution to chip densities has been "piggy-backing"
15 DIPs such that a stack of memory circuits are interconnected to emulate a
16 higher density memory circuit. Piggy-backing has resulted in several
17 problems and is seldom used anymore.

18 A more modern solution is to interconnect a stack of memory circuits
19 which are not contained in their typical package thereby effecting a greater
20 density. An example of this approach is "3-D Memory Multichip Modules"
21 from Texas Instruments. Present implementations of this approach
22 present significant problems. First, the stacked memory circuits suffer
23 from thermal problems, particularly affecting those memory circuits in the
24 middle of the stack where the heat is not adequately dissipated. Second,
25 the complexity of manufacturing the stacked memory circuits results in a
26 relatively high cost in comparison with other packaging options. Third,
27 testing of the memory circuits is difficult.

28

29 Disclosure of Invention

30 According to the present invention, a high density memory module
31 and method of forming the same is provided. The memory module has safe

1 thermal characteristics, high testability, and may be fabricated using
2 uncomplicated procedures.

3 The memory module comprises a plurality of memory subassemblies,
4 wherein each subassembly includes a memory circuit, a lead frame having
5 a plurality of leads coupled to the memory circuit, and encapsulating
6 material surrounding the memory circuit and the lead frame, such that the
7 leads extend outwardly from the encapsulating material to allow
8 convective heat transfer. Connectors couple the respective leads of the
9 memory subassemblies outside the encapsulating material to electrically
10 couple the memory circuits.

11 Advantageously, the leads extend outwardly from the encapsulating
12 material such that each of the memory circuits may dissipate heat by
13 conductive heat transfer through the leads to a convective surface. The
14 convective surface area can be adjusted for optimum heat transfer by
15 adjusting the length of the lead outside the encapsulating material.
16 Further, packaging of the memory circuit by the encapsulating material
17 may be performed such that the leads may be used for testing prior to final
18 assembly.

19 In preferred embodiments, each lead frame has an identical layout
20 such that predefined portions of the lead frame may be removed to provide
21 a unique circuit configuration corresponding to the position of the memory
22 circuit in the stack. The use of a single lead frame layout greatly simplifies
23 the construction of the memory module.

24

25 **Brief Description of Drawings**

26 Reference is now made to the following descriptions taken in
27 conjunction with the accompanying drawings, in which:

28 FIGURE 1a illustrates a perspective view of the high density memory
29 module (HDMM);

30 FIGURE 1b illustrates a pin-out for the HDMM of FIGURE 1a;

31 FIGURE 2 illustrates a schematic representation of the high density
32 memory module;

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1 FIGURE 3a illustrates a top view of a 1 M x 1 DRAM circuit showing
2 the interconnection pads;

3 FIGURE 3b illustrates a top view of a lead frame;

4 FIGURE 4a illustrates a top view of the encapsulated RAM prior to
5 assembly, showing the lead frame test points;

6 FIGURE 4b illustrates an encapsulated DRAM subassembly prior to
7 final assembly with cutaway views of the memory circuit and lead frame;

8 FIGURE 5 illustrates a bottom perspective view of the bottom header
9 of the memory module;

10 FIGURE 6 illustrates an exploded view of the memory module;

11 FIGURE 7a illustrates a top view of a 1 M x 4 DRAM circuit showing
12 the interconnection pads; and

13 FIGURE 7b illustrates a top view of a lead frame for a 1 M x 40-bit
14 HDMM.

15

16 **Best Mode for Carrying Out the Invention**

17 In referring to FIGUREs 1-7 of the drawings, like numerals are used
18 for like and corresponding parts of the various drawings.

19 FIGURE 1 illustrates a perspective view of a high density memory
20 module (HDMM). The HDMM 10 comprises a plurality of stacked
21 subassemblies 12 having protruding leads 14. Pins 16 are positioned
22 through respective aligned leads 14. The pins 16 terminate in ends 18
23 which may be attached directly to a circuit board or inserted into a socket
24 which is attached to a circuit board. A bottom header 19a and top header
25 19b are positioned at the bottom and top, respectively, of the HDMM 10.

26 Each subassembly 12 includes a memory circuit coupled to a lead
27 frame which has been encapsulated in a dielectric packaging material 13,
28 with the leads 14 protruding from the packaging material. The lead
29 frames are described in greater detail in connection with FIGURE 3b. Pins
30 16 provide electrical connections in the third (vertical) dimension to
31 distribute the appropriate signals to multiple memory circuits. The
32 subassemblies 12 may be configured in groups of eight (or nine to include a

1 parity bit) to form bytes of digital data. The number of stacked
2 subassemblies may be increased or decreased in order to provide a desired
3 word size or an alternative configuration. For purposes of illustration, the
4 HDMM will be described in connection with a 1 Mbit x 9 dynamic random
5 access memory module, although other configurations can be easily
6 designed.

7 In addition to distributing signals from the memory circuits, the lead
8 frames also provide thermal management. Heat from the memory circuits
9 is conducted to the exterior of the HDMM by leads 14, which are cooled by
10 the ambient air.

11 Using a memory circuit having dimensions of approximately 0.180 x
12 0.400 inches (.4572 x 1.016 cm), an HDMM 10 may be formed having
13 dimensions of approximately 0.340 x 0.475 x 0.435 inches (.8636 x 1.2065 x
14 1.1049 cm) using a stack of nine subassemblies 12. The HDMM achieves a
15 packaging density approaching the practical maximum possible as limited
16 by the physical size of the silicon, the lead frame and the necessary
17 encapsulation for environmental protection. Current one megabit memory
18 circuits have dimensions of approximately .243 x .115 inches (.6172 x .2921
19 cm), which significantly reduces the size of the silicon and improvements in
20 encapsulation techniques would reduce the size of the HDMM.

21 FIGURE 1b illustrates a pin-out of the HDMM 10. For the illustrated
22 embodiment of a 1 Mbit x 9 DRAM module ten address pins (A₀-A₉), nine
23 data inputs (D₁-D₉), and nine data outputs (Q₁-Q₉) are provided. CAS,
24 RAS and W provide the control signals to read and write to the HDMM.
25 V_{ss} and V_{cc} provide the power to the HDMM.

26 FIGURE 2 illustrates a schematic representation of the
27 interconnections between the memory circuits and the pins of the HDMM
28 10. The pin numbers, referenced to the pin-out of FIGURE 1b, are shown
29 parenthetically. Nine one-megabit memory circuits 20, referred to
30 individually as memory circuits 20a-20i, are used to form the HDMM 10.
31 Address pins A₀-A₉ are coupled to respective inputs for each of the memory
32 circuits 20a-20i. Similarly, V_{cc}, V_{ss}, RAS, CAS and W pins are coupled to

1 respective inputs of the memory circuits 20a-20i. The data inputs D₁-D₉
2 and data outputs Q₁-Q₉ are coupled to the data inputs (D) and data
3 outputs (Q) of respective memory chips 20a-20i. Hence, D₁ is coupled to
4 data input D of memory circuit 20a, D₂ is coupled to data input D of
5 memory circuit 20b, D₃ is coupled to data input D of memory circuit 20c,
6 and so on. Similarly, Q₁ is coupled to data output Q of memory circuit 20a,
7 Q₂ is coupled to data output Q of memory circuit 20b, and Q₃ is coupled to
8 data output Q of memory circuit 20c. Thus, for any given address, nine bits
9 of data may be either written to, or read from, the HDMM 10. Decoupling
10 capacitors 22a-d are coupled between V_{cc} and V_{ss}.

11 FIGURE 3a illustrates a top view of an exemplary memory circuit 20.
12 Signals from the memory circuit 20, as shown in connection with the
13 schematic of FIGURE 2, are available at pads 24. Connection between the
14 pads 24 and the lead frame 26 (see FIGURE 3b) may be performed by wire
15 bonding.

16 FIGURE 3b illustrates a lead frame 26 which is wire bonded to the
17 memory circuit 20 shown in FIGURE 3a. The outline of the encapsulation
18 packaging 13 and memory circuit 20 are shown for reference. In FIGURE
19 3b, the lead frame 26 is shown with the test points removed; the full lead
20 frame prior to trimming is shown in greater detail in connection with
21 FIGURE 4a. Each subassembly 12 comprises a lead frame 26 having its
22 leads 14 wire bonded to the pads 24 of the memory circuit 20. The lead
23 frame 26 is attached to the memory circuit 20 using a very thin adhesive,
24 typically an epoxy, that provides mechanical support of the lead frame 26
25 during wire bonding and also provides a low thermal impedance path for
26 heat flow from the semiconductor to the lead frame 26 which, in turn,
27 conducts heat out of the HDMM 10 through a low thermal impedance path
28 to convective surfaces for transfer into the ambient air. Typically, the lead
29 frame 26 uses a copper alloy material; however, most lead frame materials
30 will also be good heat conductors.

31 Importantly, a single lead frame configuration may be used in
32 connection with any one of the subassemblies in the HDMM, regardless of

1 its position in the stack, thereby reducing the complexity of manufacture.
2 The data input D of the memory circuit is coupled to a signal pad 28 which
3 is electrically coupled via removable connections 30 to each of the leads 14
4 associated with pins D₁-D₉. To configure the lead frame 26 for a particular
5 subassembly level, all but one of the removable connections 30 are
6 removed. For example, the lead frame 26 coupled to memory circuit 20a
7 will have the removable connections 30 associated with leads D₂-D₉
8 removed. Similarly, the lead frame 26 includes a signal pad 32 coupled to
9 the data output Q of the memory circuit 20. The signal pad 32 is coupled to
10 the leads 14 associated with data outputs Q₁-Q₉ via removable connections
11 34. Again, for a particular subassembly level, the removable connections
12 34 for all but one of the leads 14 associated with Q₁-Q₉ are removed. Thus,
13 for memory circuit 20a, all removable connections 34 are removed except
14 for the connector associated with the Q₁ lead. Hence, memory circuit 20a
15 has its data input pad D coupled to the D₁ lead and has its data output pad
16 Q coupled to the Q₁ lead. The subassemblies 12 are marked either during
17 or after encapsulation to identify the unique data input/output
18 configuration.

19 In the preferred embodiment, the leads 14 are spaced on 0.025 inch
20 (0.0635 cm) centers outside of the encapsulating package and configured as
21 shown with holes 37 located to provide a three-dimensional interconnect
22 via pins 16.

23 Each subassembly 12 should undergo a complete electrical test and
24 subsequent burn-in after encapsulation. FIGURE 4a illustrates the
25 encapsulated memory circuit, showing the extended lead frame test points.
26 Prior to encapsulation, the lead frame 26 has extended leads 36 with test
27 points 38. The encapsulation process forms the subassemblies 12 with
28 leads 14 still connected to extended leads 36. The extended leads are
29 encapsulated in the secondary package 40 with the test points 38 exposed.
30 Hence, at this point in the fabrication process, the memory circuits may be
31 easily tested.

1 As shown in FIGURE 4b, the subassemblies 12 are separated from
2 the secondary package 40 prior to assembly of the HDMM 10. FIGURE 4b
3 illustrates a cutaway view showing the memory circuit 20 and lead frame
4 26 encapsulated within the package 13.

5 FIGURE 5 illustrates a bottom view of the bottom header 19a. The
6 bottom header includes the four capacitors 22a-d (shown in FIGURE 2)
7 coupled between the pins associated with V_{cc} and V_{ss} .

8 FIGURE 6 illustrates an exploded view of the HDMM 10 to show the
9 assembly of the various parts. The subassemblies 12 are stacked, with
10 each subassembly uniquely addressed using removable connections 30 and
11 34 such that each subassembly has a unique data input/output pin-out.
12 The bottom header is placed at the bottom of the stack of subassemblies,
13 with the capacitors 22a-d disposed away from the subassemblies, (i.e.,
14 towards the circuit board) and the top header 19b is disposed above the
15 stack of subassemblies 12. The pins 16 are disposed through the vertically
16 aligned leads 14 and the holes in the headers 19a-b. A thin adhesive is
17 used between each subassembly 12. Subsequent to placing the pins
18 through the leads, the adhesive is cured and a reflow solder process is used
19 on electrical joints using a high temperature solder to complete the
20 assembly.

21 In the preferred embodiment, the bottom header 19a is fabricated
22 from sheets of copper-clad high-temperature plastic that are subsequently
23 drilled and etched or molded from high-temperature plastic and selectively
24 copper-plated to provide the decoupling capacitor mounting pads and
25 annular rings at each of the thirty-six holes. The top header 19b is
26 fabricated similarly, but without the capacitor mounting pads.

27 Each of the individual components (headers 19a-b, unique
28 subassemblies 12, and capacitors 22) may be packaged in embossed tape on
29 reels to enhance material handling accuracy and to ease presentation to
30 the assembly equipment. In the preferred embodiment, the assembly
31 process successively places the components onto the thirty-six individual
32 pins that are cut from individual rolls of round wire. The HDMM 10 may

1 be assembled in an inverted position such that the coined ends of the pins
2 may more easily align with the hole pattern of each subassembly 12 in the
3 stack.

4 After cleaning, each HDMM 10 may be electrically tested and placed
5 in a temperature-cycle burn-in oven for final conditioning.

6 FIGUREs 7a-b illustrate a pin-out for a 1 M x 4-bit memory circuit
7 and a lead frame configuration for implementing a 1 M x 40 bit memory,
8 respectively. The 1 M x 4-bit memory circuit 42 comprises ten address
9 lines (A_0 - A_9), four data input/output signals (DQ_1 - DQ_4), power signals (V_{cc} ,
10 V_{ss}) and control signals (\overline{CAS} , \overline{RAS} , \overline{OE} and \overline{W}).

11 Each of the data input/output signals of the memory circuit 42 is
12 coupled to an associated signal pad on the 1 megabit x 40 lead frame 44.
13 Hence, input/output DQ_1 of memory circuit 42 is coupled to signal pad 46,
14 input/output DQ_2 is coupled to signal pad 48, input/output DQ_3 is coupled
15 to signal pad 50 and input/output DQ_4 is coupled to signal pad 52. Each of
16 the signal pads 46-52 are coupled to a respective set of ten leads 14. Signal
17 pad 46 is coupled to ten leads 14, labeled $DQ_1(1)$ - $DQ_1(10)$, via removable
18 connections 34 as described in connection with FIGURE 3b. Similarly,
19 signal pad 48 is coupled to leads 14 labeled $DQ_2(1)$ - $DQ_2(10)$, signal pad 50
20 is coupled to leads 14 labeled $DQ_3(1)$ - $DQ_3(10)$ and signal pad 52 is coupled
21 to leads 14 labeled $DQ_4(1)$ - $DQ_4(10)$. The remaining connections between
22 memory circuit 42 and lead frame 44 are the same as described in
23 connection with FIGURE 3b.

24 For each subassembly level of the 1 M x 40 HDMM, the associated
25 lead frame 44 will be uniquely identified by removing all but one of the
26 removable connections 34 for each set of leads DQ_1 - DQ_4 . For example, at
27 the first level, leads $DQ_1(1)$, $DQ_2(1)$, $DQ_3(1)$ and $DQ_4(1)$ will each be
28 coupled to their respective signal pads while the remaining leads will be
29 decoupled by removing removable connections 34. For a 1 M x 40 HDMM,
30 ten levels of subassemblies will be needed.

31 While the previous embodiments described a 1 Mbyte DRAM module,
32 other configurations could be similarly designed. For example, for a 1 M x

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1 16 bit HDMM, the lead frame 26 could provide sixteen data input leads
2 and sixteen data output leads (or eighteen input/output leads using byte
3 parity) using 1 M x 1-bit memory circuits. Further, the address range of
4 the HDMM could be increased by using a higher density memory circuit
5 (for example, a 4 Mbit x 1 memory circuit) and providing additional
6 address leads or by using additional subassembly chip select signals.
7 Further, the HDMM could be used with other memory technologies such as
8 static RAM and flash memory circuits.

9 Various changes, substitutions and alterations can be made herein
10 without departing from the scope of the invention as defined by the
11 appended claims.

CLAIMS

3 1. A memory module (10) comprising a plurality of memory
4 subassemblies (12), each subassembly (12) comprising (i) a memory circuit
5 (20), (ii) a lead frame (26) having a plurality of thermally and electrically
6 conductive leads (14) with selected leads (14) electrically coupled to said
7 memory circuit (20) and non-selected leads (14) electrically isolated from
8 said memory circuit (20), and (iii) an encapsulating material (13)
9 surrounding said memory circuit (20) and a portion of lead frame (26)
10 wherein said leads (14) extend outwardly from said encapsulating material
11 (13), said memory module (10) further comprising electrical connectors (16)
12 coupled to portions of said leads (14) outside of said encapsulating material
13 (13), characterized in that:

14 each of said leads (14) provides conductive heat transfer from said
15 memory circuit (20) to an area outside said encapsulating material (13) and
16 convective heat transfer from the portions of said leads (14) extending
17 outside of said encapsulating material (13); and

18 at least one of said selected leads (14) is selectively coupled to said
19 memory circuit (20).

21 2. A memory module (10) comprising a lead frame (26), a memory
22 circuit (20) and an encapsulating material (13), said lead frame (26)
23 comprising (i) a plurality of first leads (14) electrically coupled to said
24 memory circuit (20) and extending outside said encapsulating material
25 (13), (ii) a plurality of second leads (14) extending outside said
26 encapsulating material (13), and (iii) a plurality of conductive surfaces
27 (28,32) electrically coupled to said memory circuit (20) and completely
28 surrounded by said encapsulating material (13), characterized by:

29 said lead frame (26) further comprising removable connectors (30,34)
30 for selectively coupling said second leads (14) to said conductive surfaces
31 (28,32).

1 3. A method of forming a memory module (10), comprising the steps
2 of (i) providing a plurality of lead frames (26) containing leads (14), (ii)
3 electrically coupling a plurality of memory circuits (20) to respective lead
4 frames (26), (iii) adhering said memory circuits (20) to said respective lead
5 frames (26), (iv) encapsulating said coupled memory circuits (20) and
6 portions of said respective lead frames (26) to form memory subassemblies
7 (12) such that outer ends of leads (14) extend out from an encapsulating
8 material (13), and (v) electrically coupling said subassemblies (12) by
9 interconnecting said outer ends of leads (14), characterized by:

10 configuring a plurality of identical lead frames (26) in step (i) such
11 that each of said plurality of lead frames (26) provides a unique
12 input/output data path for the respective memory circuit (20).

13

14 4. A three-dimensional memory module (10) comprising (I) a
15 plurality of horizontally-oriented, vertically-stacked memory subassemblies
16 (12), each memory subassembly (12) comprising (i) a memory circuit (20)
17 comprising a plurality of bonding pads (24) for receiving data input signals,
18 address signals, control signals and power supply voltages, and for sending
19 data output signals, (ii) a lead frame (26) formed of thermally and
20 electrically conductive material comprising a plurality of outwardly
21 extending leads (14) wherein selected leads (14) are electrically coupled to
22 said pads (24) whereas non-selected leads (14) are electrically isolated from
23 said pads (24), (iii) a mechanical coupling element between said memory
24 circuit (20) and said lead frame (26), and (iv) a dielectric material (13)
25 surrounding and encapsulating said memory circuit (20) and a portion of
26 said lead frame (26) wherein the unencapsulated portion of said lead frame
27 (26) includes outer portions of leads (14), said outer portions of leads (14)
28 protruding from said dielectric material (13) and providing convective
29 surface areas to ambient air outside said dielectric material (13), wherein
30 said lead frames (26) are positioned so that said outer portions of leads (14)
31 are aligned in vertical columns, and (II) a plurality of separate, spaced
32 vertically-oriented electrical connectors (16) positioned outside said

1 dielectric material (13) wherein each electrical connector (16) electrically
2 couples the outer portion of each lead (14) in a single vertical column of
3 leads (14) without electrically coupling the outer portion of any leads (14)
4 outside said single vertical column, characterized in that:

5 a thermal coupling element is between said memory circuit (20) and
6 said lead frame (26);

7 said lead frame (26) provides a low thermal impedance path that
8 allows said memory circuit (20) to dissipate heat by conductive heat
9 transfer through said thermal coupling element into said lead frame (26)
10 within said dielectric material (13) and through said lead frame (26) within
11 said dielectric material (13) to the convective surface areas of said outer
12 portions of leads (14);

13 said lead frames (26) are configured so that each data input pad (24)
14 of each memory circuit (20) is the only data input pad (24) in the memory
15 module (10) which is electrically coupled to a selected electrical connector
16 (16), thereby providing each memory subassembly (12) with a unique data
17 input configuration corresponding to the position of the memory
18 subassembly (12) in the stack; and

19 said lead frames (26) are configured so that each data output pad (24)
20 of each memory circuit (20) is the only data output pad in the memory
21 module (10) which is electrically coupled to a selected electrical connector
22 (16), thereby providing each memory subassembly (12) with a unique data
23 output configuration corresponding to the position of the memory
24 subassembly (12) in the stack.

1 5. The memory module (10) of claim 4 wherein:
2 said outer portions of leads (14) of each lead frame (26) have identical
3 layouts, said dielectric materials (13) have identical layouts, and said
4 memory subassemblies (12) are stacked adjacent to one another;

5 said electrical connectors (16) are formed of thermally and electrically
6 conductive metal, provide convective surface areas to said ambient air, and
7 are electrically and thermally coupled to said vertical columns of leads (14);

8 the entire surfaces of said outer portions of leads (14) and the entire
9 surfaces of said electrical connectors (16) between the top and bottom of the
10 stack are convective surface areas; and

11 said lead frame (26) is formed with opposing major surfaces parallel
12 to one another, said memory circuit (20) is disposed over said leads (14),
13 said mechanical coupling element mechanically couples said memory
14 circuit (20) to portions of said leads (14) beneath said memory circuit (20),
15 said thermal coupling element thermally couples said memory circuit (20)
16 to portions of said leads (14) beneath said memory circuit (20); and metallic
17 bonds electrically couple said pads (24) to said selected leads (14).

18

19 6. The memory module (10) of claim 4 wherein:

20 said memory circuit (20) is disposed over said leads (14);

21 said mechanical coupling element mechanically couples said memory
22 circuit (20) to portions of said leads (14) beneath said memory circuit (20);

23 said thermal coupling element thermally couples said memory circuit
24 (20) to portions of said leads (14) beneath said memory circuit (20); and

25 metallic bonds electrically couple said pads (24) to said selected leads
26 (14).

27

28 7. The memory module (10) of claim 6 wherein:

29 said lead frame (26) consists of said leads (14);

30 said leads (14) have flat and parallel top and bottom surfaces within
31 said dielectric material (13);

1 said memory circuit (20) is formed with a flat bottom surface facing
2 said leads (14) and opposite said pads (24); and

3 said mechanical coupling element adhesively connects the bottom
4 surface of said memory circuit (20) to the top surfaces of said leads (14)
5 therebeneath.

6

7 8. The memory module (10) of claim 4 wherein all low thermal
8 impedance paths between said memory circuit (20) and said ambient air
9 must include said thermal coupling element and said lead frame (26).

10

11 9. The memory module (10) of claim 4 wherein:

12 said memory circuit (20) and said lead frame (26) are the only
13 thermally conductive materials in contact with said thermal coupling
14 element; and

15 said lead frame (26) is the only thermally conductive material both
16 within and in contact with said dielectric material (13).

17

18 10. The memory module (10) of claim 4 wherein said mechanical
19 and thermal coupling elements are a single adhesive material in full
20 surface contact with one surface of said memory circuit (20).

21

22 11. The memory module (10) of claim 4 wherein:

23 all electrical interconnections between said pads (24) and circuitry
24 outside said dielectric material (13) must include said selected leads (14);
25 in each of said memory subassemblies (12), excluding said power
26 supply pads (24), each of said pads (24) is coupled to a single selected lead
27 (14) and each of said selected leads is coupled to a single pad (24);

28 said memory subassemblies (12) have identical power supply, control
29 signal and address signal configurations, and said electrical connectors (16)
30 connect all power supply voltages, control signals and address signals in
31 common among said memory circuits (20);

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1 some but not all of said selected leads (14) in a given memory
2 assembly (12) include a removable connection surrounded by said
3 encapsulating material (13); and

4 each of said non-selected leads (14) in a given memory subassembly
5 (12) is electrically coupled to a single electrical connector (16) which is
6 electrically coupled to a single pad (24) on a single memory circuit (20) in
7 another memory subassembly (12), said single pad (24) functioning as at
8 least one of said data input pad (24) or said data output pad (24).

9

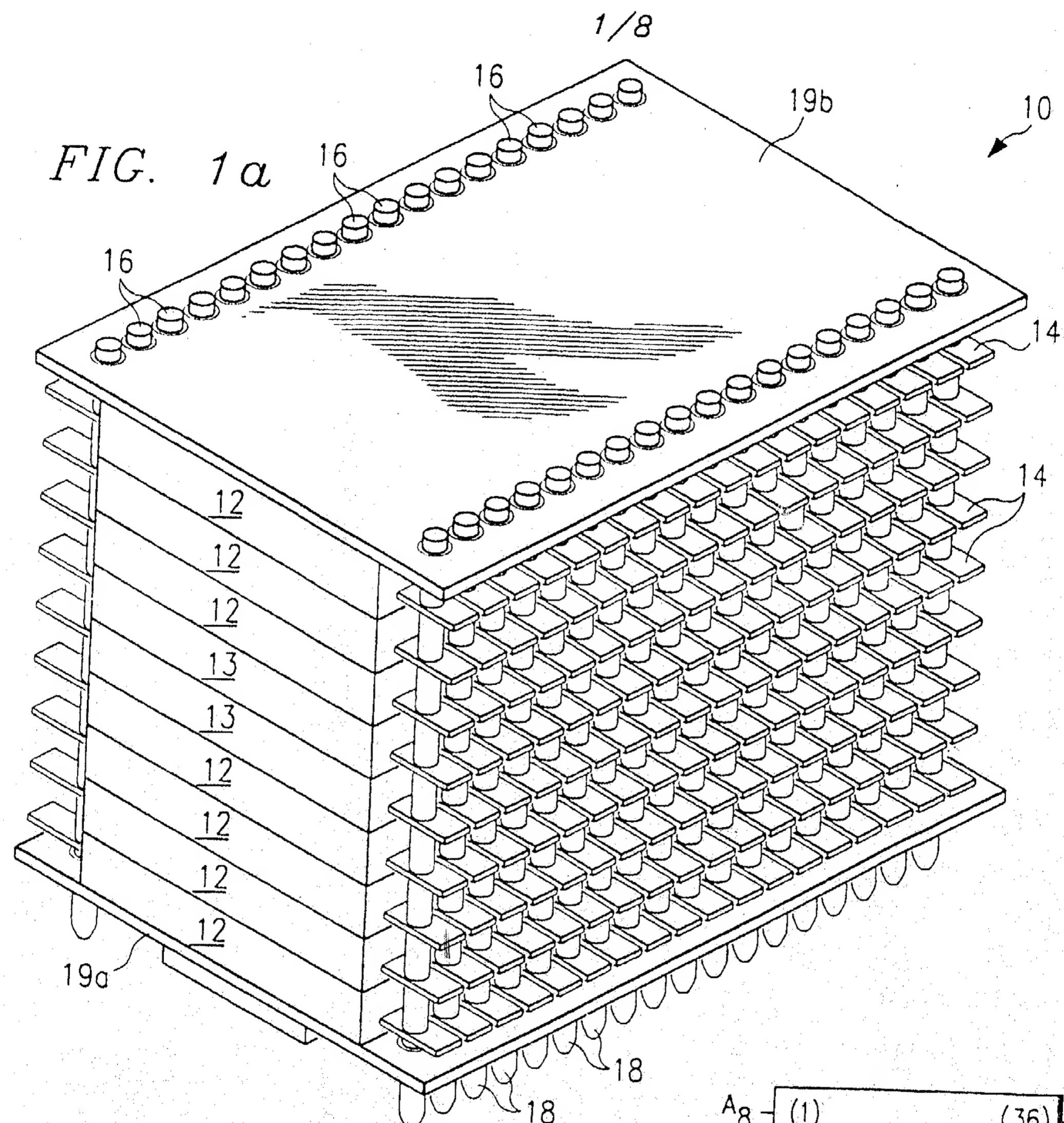
10 12. The memory module (10) of claim 4 wherein:
11 said unique data input and data output configurations for said
12 memory circuit (20) are provided by several opened connections on the
13 encapsulated portion of said lead frame (26);

14 each non-selected lead (14) is rendered electrically isolated from said
15 pads (14) by a single opened connection;

16 said data input pad (24) is electrically coupled to a single selected
17 lead (14) which includes a removable connection (30);

18 said data output pad (24) is electrically coupled to a single selected
19 lead (14) which includes a removable connection (34); and

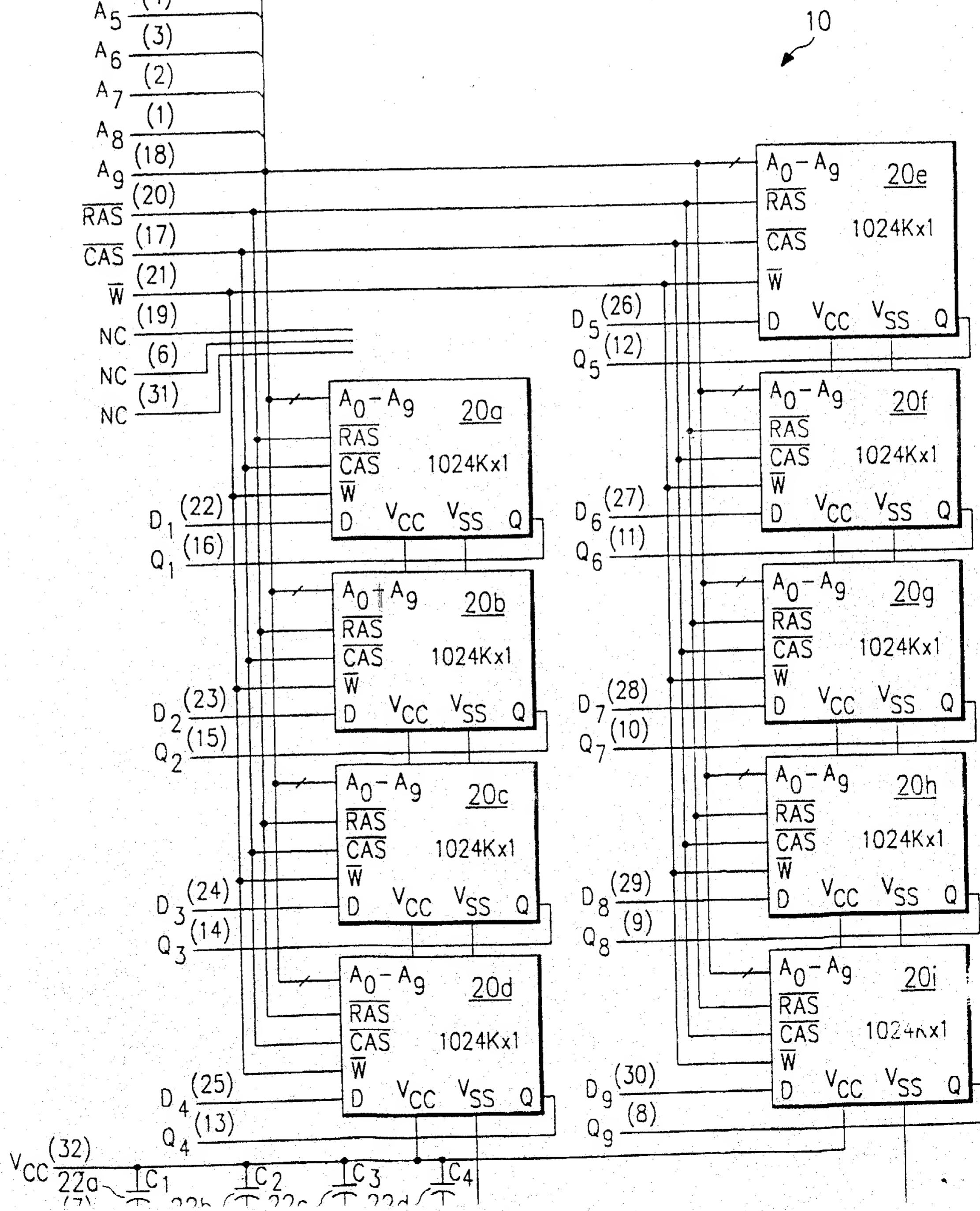
20 each of said lead frames (26) has a uniquely positioned removable
21 connection (30,34) included in one but not all of said selected leads (14).

*FIG. 1b*

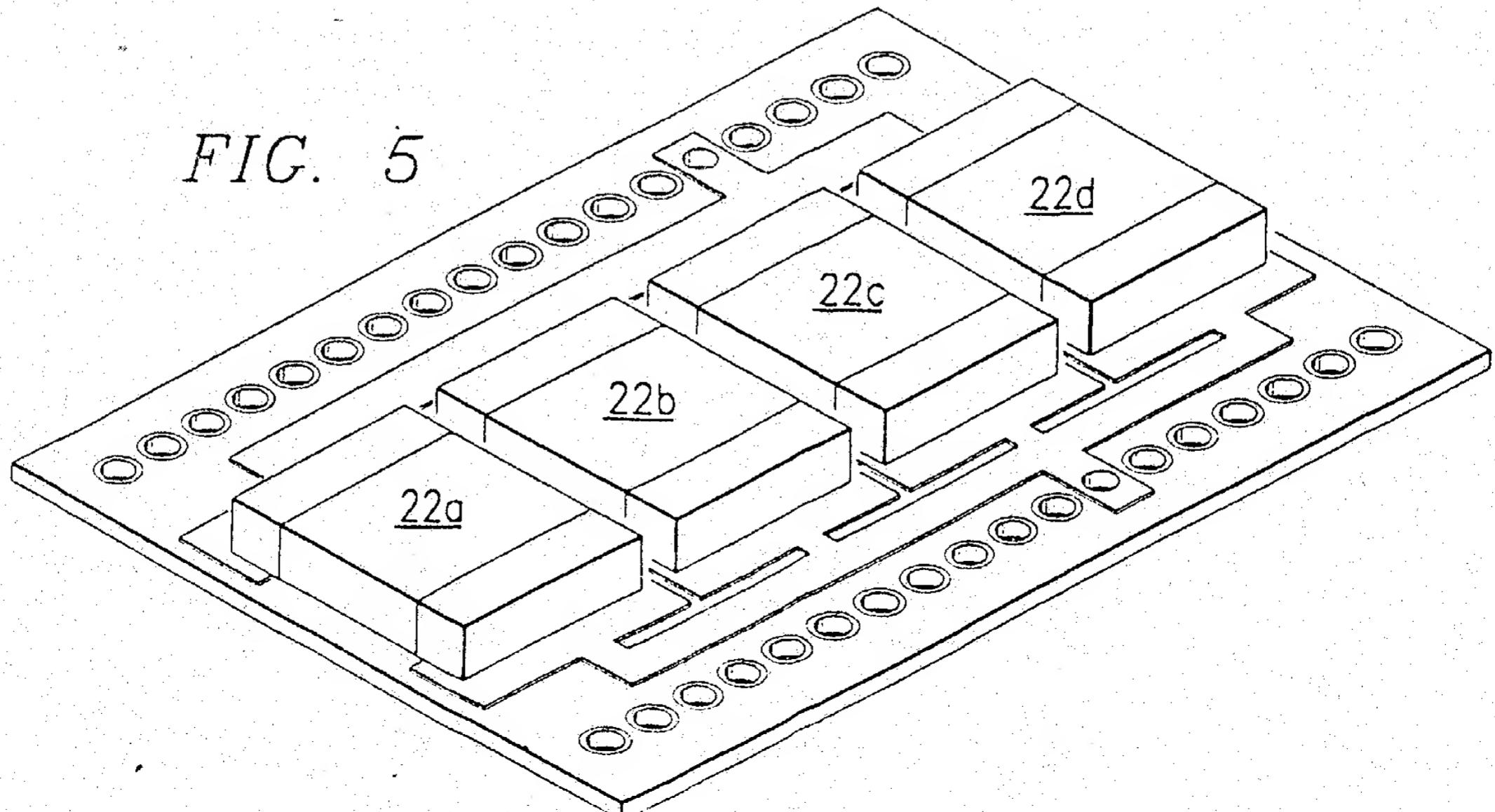
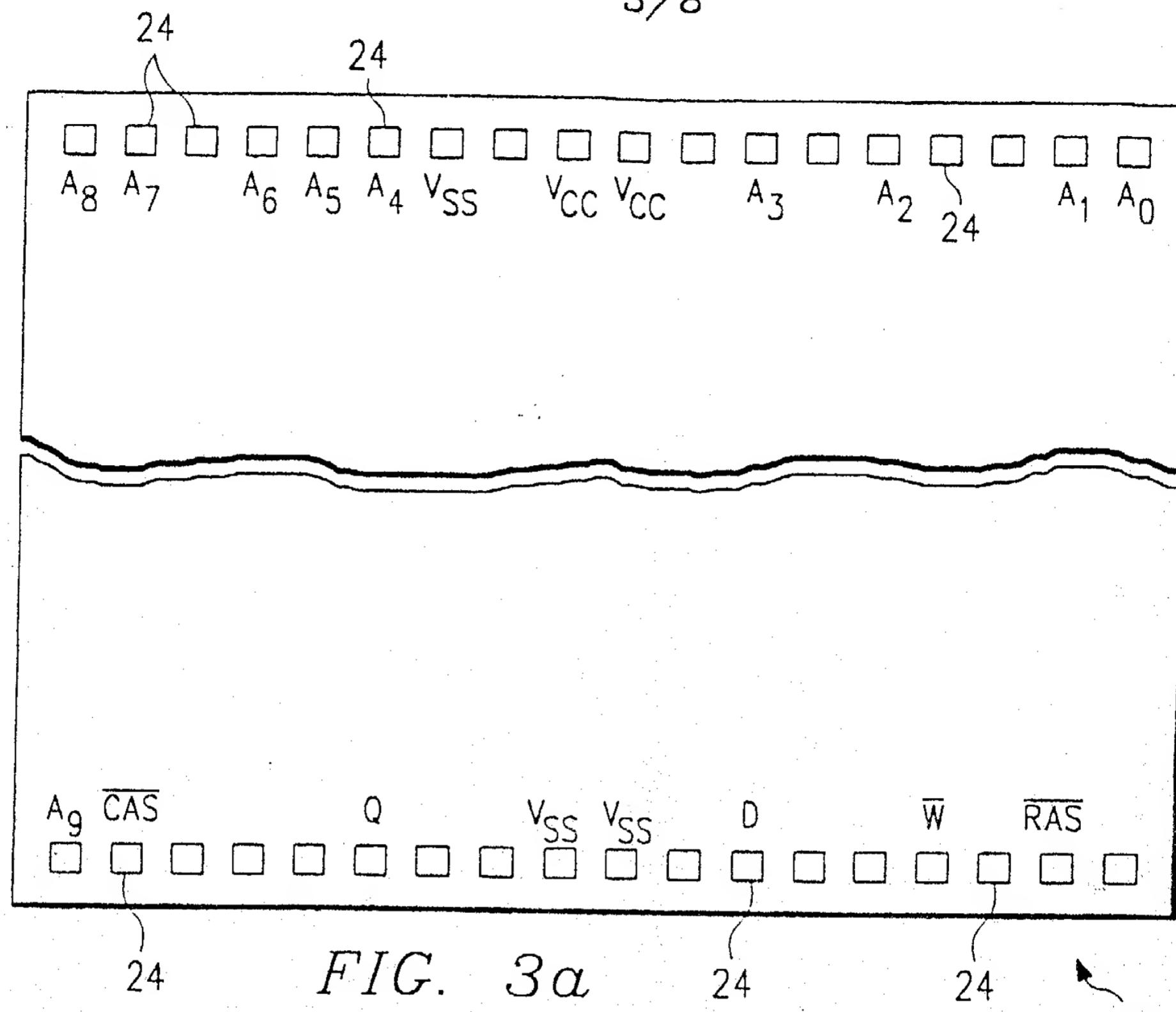
| (1) | (36) |
|------------------|-----------|
| A_8 | A_0 |
| A_7 | A_1 |
| A_6 | A_2 |
| A_5 | A_3 |
| A_4 | V_{CC} |
| NC | NC |
| V_{SS} | D_9 |
| Q_9 | D_8 |
| Q_8 | D_7 |
| Q_7 | D_6 |
| Q_6 | D_5 |
| Q_5 | D_4 |
| Q_4 | D_3 |
| Q_3 | D_2 |
| Q_2 | D_1 |
| Q_1 | \bar{W} |
| \overline{CAS} | RAS |

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FIG. 2

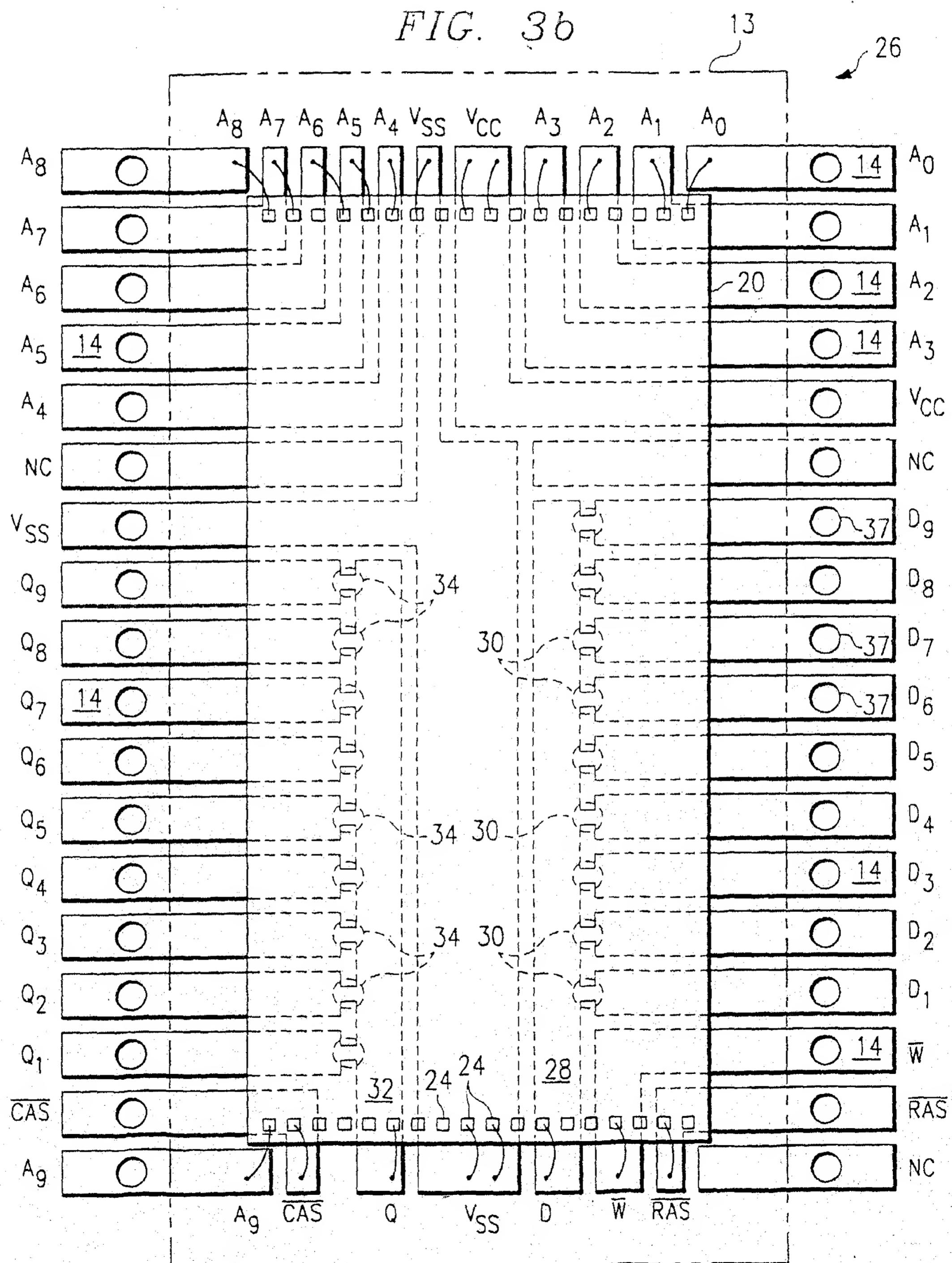


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FIG. 36



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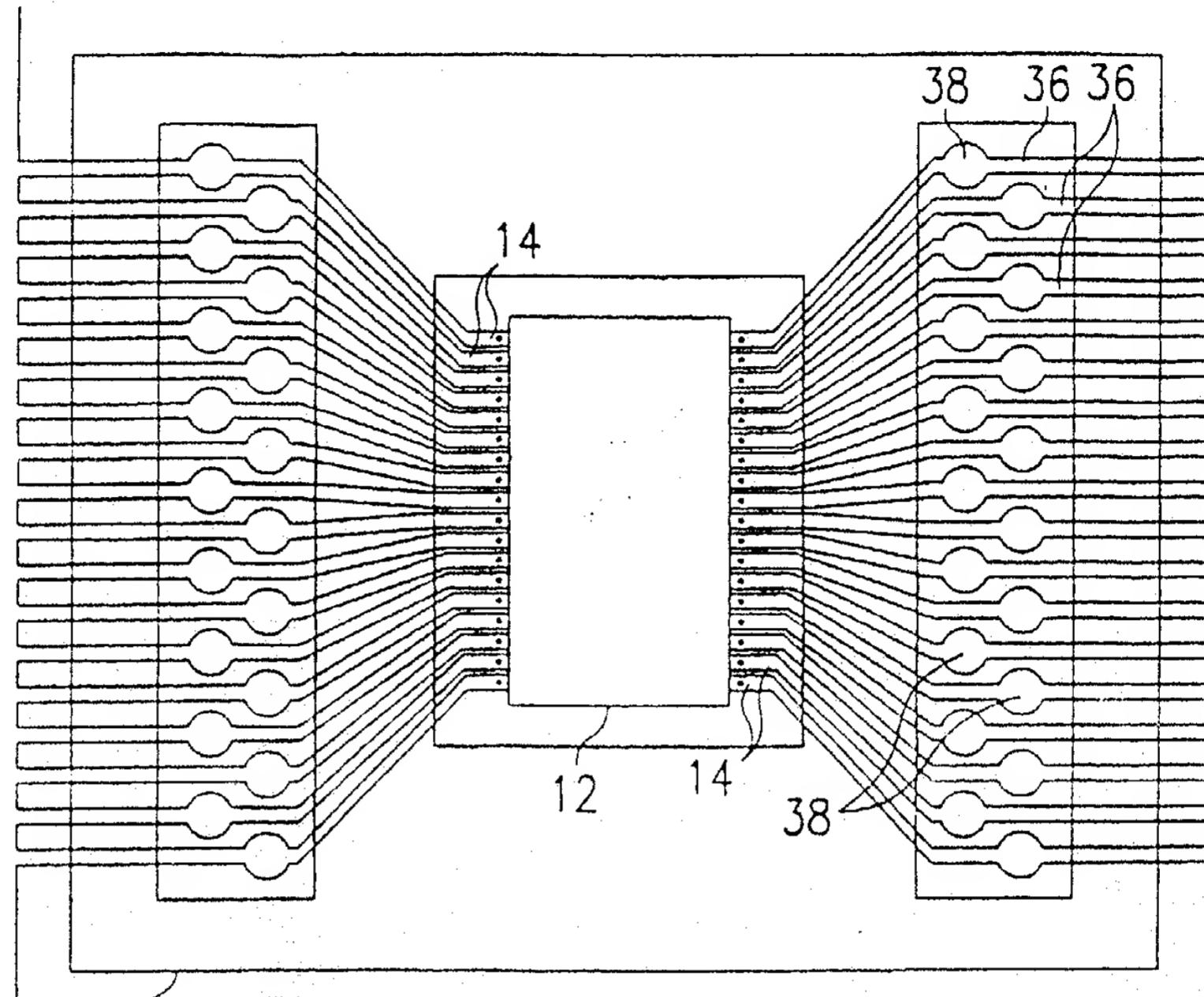


FIG. 4a

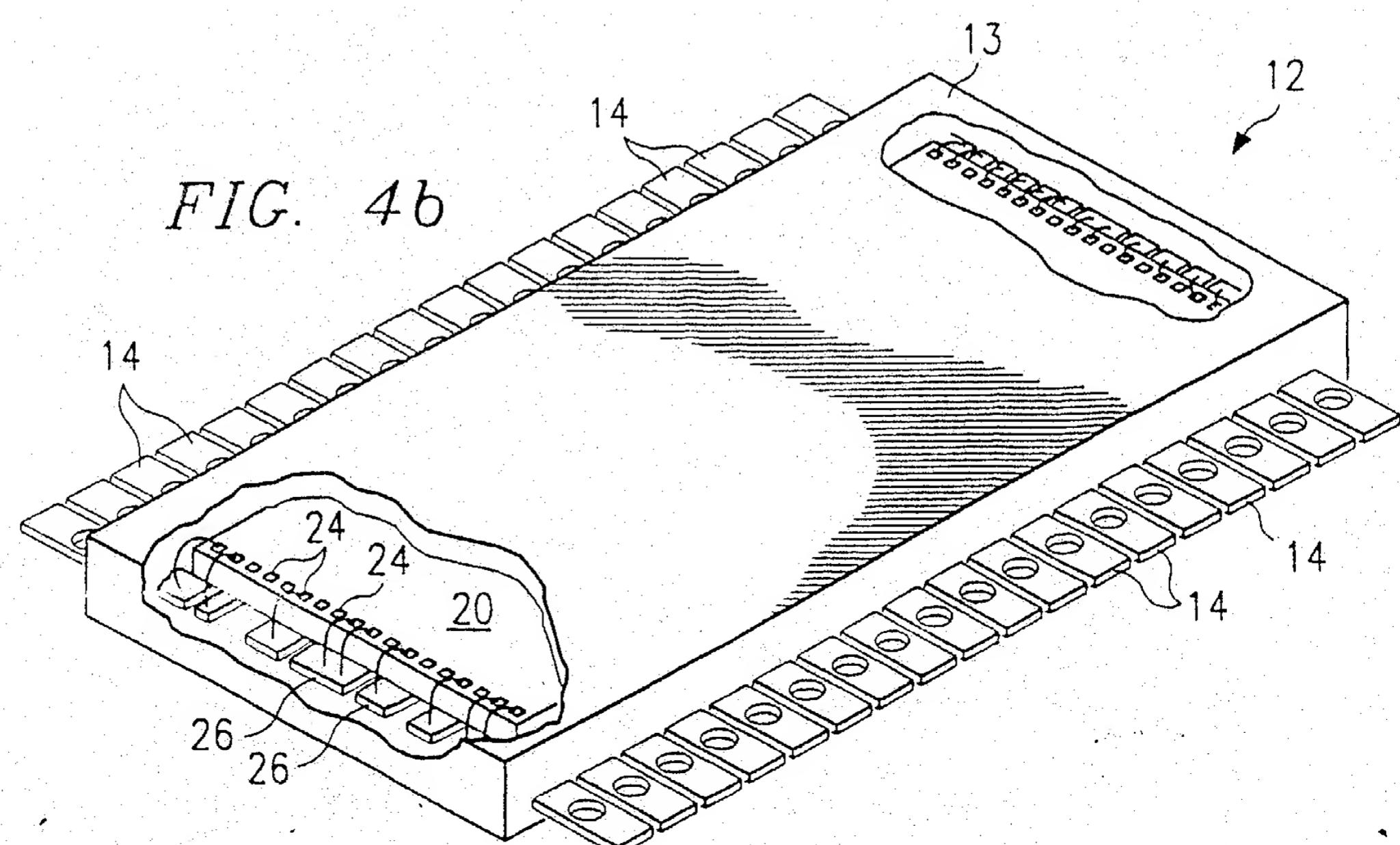
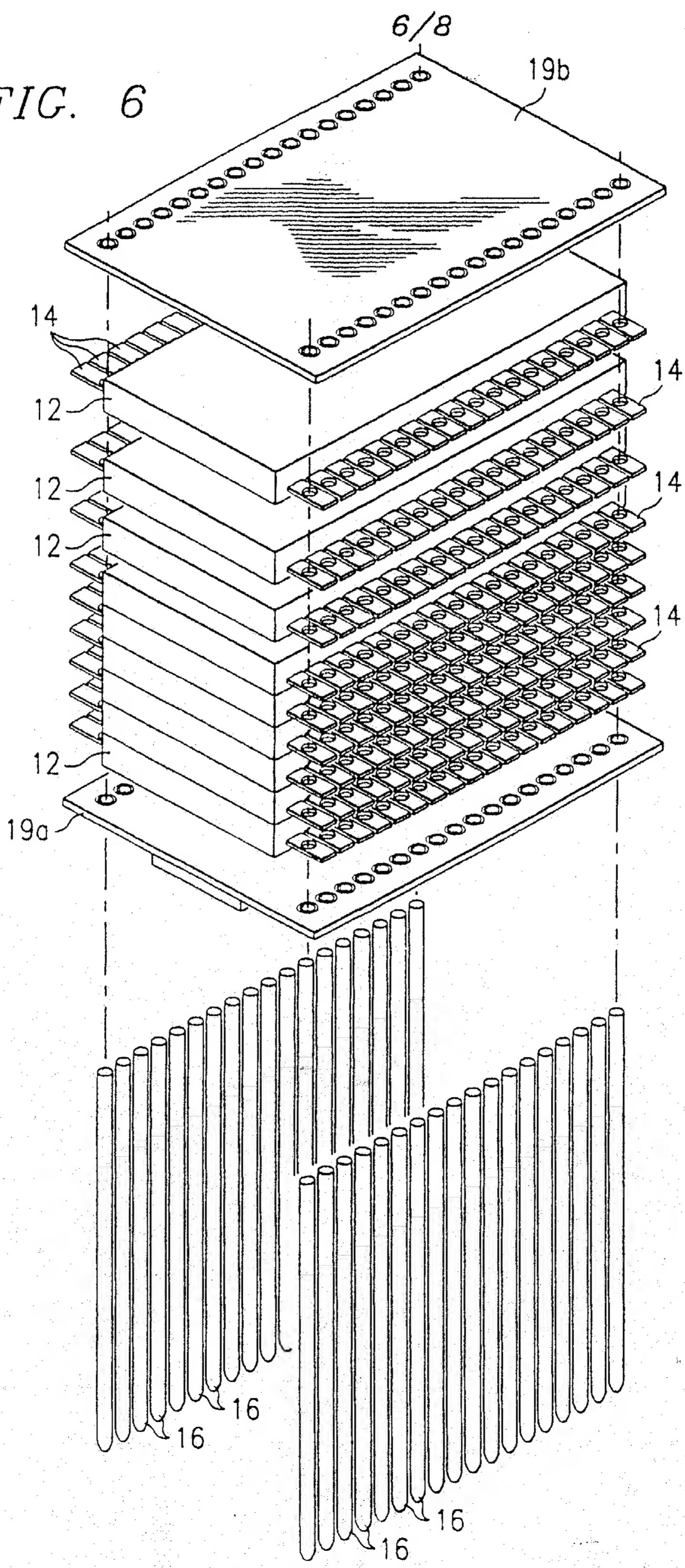


FIG. 4b

FIG. 6



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42

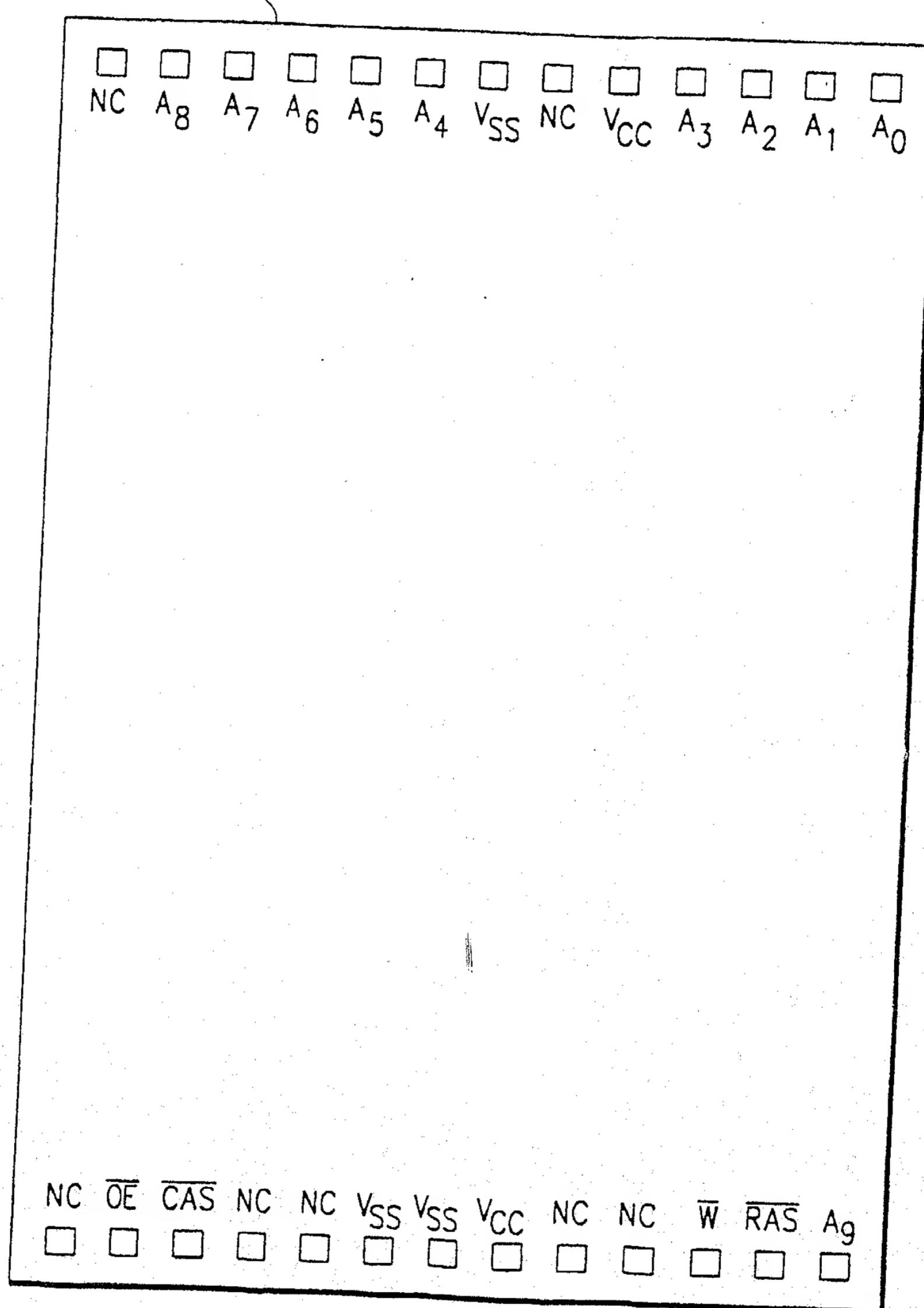


FIG. 7a

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FIG. 7b

